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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Group Art Unit: 2812)
Applicant: Inao Toyoda et al)
Serial No. 10/613,192)
Filing Date: July 3, 2003)
Title: Photo Sensing Integrated)
Circuit Device and Related)
Circuit Adjustment)
Docket No.: 4041P-000005/DVA)

RESPONSE TO
NOTICE OF ALLOWABILITY

Notice of Allowance dated 02/17/2005

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

EV 570 162 851 US


Sir:

Applicants acknowledge receipt of the Notices of Allowance and Allowability in connection with the above-identified patent application and have noted that the Examiner indicated that "None" of the foreign priority documents for which a priority is made in this application, have been received (4.c). Applicants respectfully wish to point out that certified copies of the Japanese priority documents (Japanese Application Nos. 9-92482, 9-92481 and 9-96050) were submitted in the parent application, U.S. Serial No. 09/057,561, and therefore Box 4.a.2 should have been checked to indicate the same.

Respectfully submitted,
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Date: 2/25/05


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